IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	Date: January 13, 2009
Robert T. BAILIS et al.	Confirmation No: 5286
Serial No: 10/016,449	Group Art Unit: 2117
Filed: December 10, 2001	Examiner: John J. Tabone, Jr.

For: METHOD AND SYSTEM FOR USE OF A FIELD PROGRAMMABLE GATE ARRAY(FPGA) FUNCTION WITHIN AN APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC) TO ENABLE CREATION OF A DEBUGGER CLIENT WITHIN THE ASIC

Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT IN RESPONSE TO OCTOBER 16, 2008 OFFICE ACTION

Sir:

In response to the Office Action of October 16, 2008, Applicant submits the following amendments and remarks:

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 5 of this paper.